

**UNITED STATES DISTRICT COURT  
EASTERN DISTRICT OF NEW YORK**

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VEECO INSTRUMENTS INC.,

Plaintiff,

v.

SGL CARBON, LLC et al.,

Defendants.

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) Civil Action No. 1:17cv2217 (PKC)

)  
) DECLARATION OF  
) DR. ALEXANDER GLEW  
) IN SUPPORT OF PLAINTIFF’S  
) MOTION FOR PRELIMINARY  
) INJUNCTION  
)  
)  
)

I, Dr. Alexander Glew, hereby declare and state as follows:

1. I have been retained by Plaintiff Veeco Instruments Inc. (Veeco) to offer technical analysis and opinions regarding various issues relevant to this action, including the infringement of the patent-in-suit, U.S. Patent No. 6,726,769 (the ’769 patent). I have personal knowledge of the facts stated herein, and if called to testify as a witness, I could and would testify competently thereto.

2. I received a Bachelor of Science degree in Mechanical Engineering from University of California, Berkeley in 1985; a Master of Science degree in Mechanical Engineering from University of California, Berkeley in 1987; a Master of Science in Materials Science and Engineering from Stanford University in 1995; and Doctor of Philosophy degree in Materials Science and Engineering from Stanford University in 2003. A copy of my Curriculum Vitae (“CV”) is attached to this report as Exhibit 1 Veeco0001955-01974 (Alexander D. Glew, Ph.D., P.E. Curriculum Vitae).

3. The subject matter of my doctoral dissertation at Stanford University related to chemical vapor deposition (“CVD”) of dielectric films. CVD generally consists of mixing two or more gases in a process reactor or chamber, and having the gases meet on the surface of a substrate to deposit a thin film. Many of the CVD films that I worked on were deposited on undoped silicon glass ( $\text{SiO}_2$ ), and boron and phosphorous doped glass. The CVD equipment to be manufactured in this case was to mix various gaseous chemicals and to deposit the chemicals onto glass to produce certain types of specialty glasses. For my doctoral dissertation, I constructed a CVD reactor. Then, I developed CVD processes for certain low k dielectric films such as diamond like carbon and fluorinated amorphous carbon. Further, I characterized those thin films for their engineering properties, optical, electrical, and mechanical. Also, I analyzed the chemical composition of the thin films.

4. From 1987-1997, I was employed by Applied Materials, Inc. (“Applied Materials”), one of the world’s largest and most advanced manufacturers of, among other things, CVD-related equipment. I was hired by the CVD division. The first process tool that I worked on was the Precision 5000 CVD tool. It was the first cluster tool, a tool with multiple CVD processing chambers. Because this tool demonstrated the major advance in tool architecture, multiple chambers attached to a central vacuum load lock chamber, resulting in the ability to process one workpiece at a time instead of in batch, it was eventually placed in the Smithsonian Institute, Natural History Museum.

5. Subsequent to being a Systems Engineer, from approximately 1989-1991, I was an Engineering Manager at Applied Materials responsible for customer engineering specials (“CES”). This included customization of equipment to meet customer requests and specifications. The CES requests were diverse and covered nearly all aspects of the equipment,

ranging from modifying process chambers, gas panels, wafer handlers/robotics, wafer storage elevators, sensors, vacuum systems, framing, and other. We worked on very tight schedules, and exercised disciplined project management. If our engineering work was not completed on time, and the materials not procured, then it would hold up the shipment of a multi-million dollar CVD process tool. Because we exercised disciplined project management, such delays rarely happened. We also had to accurately estimate the cost of our work, materials and labor, because the CES projects were billed to the customer.

6. Next, I was the manager of the engineering design and support group for the CVD division of Applied Materials. In this capacity, I was in charge of all of the designers and drafters, generating all of the engineering drawings, and reviewing all of the engineering design work. I am intimately familiar with computer aided design (“CAD”) and engineering documentation.

7. In the early 1990s, I was awarded the position of Core Technologist (one of only 15 in Applied Materials). My area of expertise was gas and chemical systems and components. The gas and chemical systems largely delivered ultra-high purity fluids to the process chambers and reactors. Components used in the systems included the following: valves, flow controllers, pressure regulators, filters, purifiers, pressure transducers and related devices, and systems as a whole. As a core technologist, I was responsible for consulting with different divisions during the design of new products, testing fluid delivery components, reviewing invention disclosures, and reviewing papers written by Applied Materials personnel, holding meetings across the divisions for workers in the field, setting technology trends with suppliers, and reviewing technology trends with customers. Our different divisions included product lines such as at least CVD, ETCH, CMP, implant, TFT, and more. I also represented the company at industry

consortium meetings. The core technology group met monthly with the president or other senior executives of the company.

8. From 1994-1996, I managed a project funded by SEMATECH<sup>1</sup> that I proposed to its factory working group. These efforts resulted in the publication of two SEMATECH technology transfer standards. The goal of this project was to develop industry standard methods to determine the effects of trace chemicals and contamination on semiconductor processing and on semiconductor equipment reliability. As part of this project, I designed, built, and tested gas delivery systems, including the components contained therein, such as filter cartridges or assemblies, flow controllers, valves, and pressure regulators, and tested them to failure. Approximately 90% of wafer yield loss is from particles, so the industry was very interested in the particle effect of the chemical delivery system. I also tested the effect of micro-contamination in the process gas stream on tungsten CVD deposition and on metal etching. In some of the tests, we introduced controlled amounts of fluid into corrosive gas streams, and then measured the effect on system reliability, including particle generation.

9. As part of the SEMATECH project, we studied the effects of trace chemical contamination on tungsten CVD processing and on metal etching. We introduced trace chemicals into a standard process, measured the amounts of chemical in the process chamber by residual gas analyzer (RGA), and then measured the resulting film quality and properties by multiple techniques, and incorporation of the trace chemicals into the deposited layers.

10. From 1994-1997, I was a CVD Supplier Quality Engineering Manager at Applied Materials. During this time, I was the engineering manager responsible for the suppliers of the components of the fluid delivery systems, such as valves, flow controllers, pressure regulators,

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<sup>1</sup> SEMATECH stands for “Semiconductor Manufacturing Technology”, a non-profit consortium that performs research into semiconductor manufacturing.

filters, purifiers, pressure transducers and related devices, and systems as a whole. I tested and evaluated fluid delivery components. I both supervised and personally conducted this testing.

11. Since leaving Applied Materials in 1997 and until the present, I have served as president of Glew Engineering Consulting, Inc. ("Glew Engineering") of Mountain View, California. Glew Engineering provides consulting and engineering services relating to various technology or engineering areas, including CVD technology. My responsibilities at Glew Engineering include acting as a consultant and as a principal managing the company.

12. I am or have been a member of a number of professional organizations including: American Society of Mechanical Engineers, Materials Research Society, IEEE (Institute of Electrical and Electronics Engineers). Glew Engineering is an Affiliate Member of Semiconductor Equipment and Materials Institute (SEMI). In addition to being a member of these professional organizations, I have served on committees at SEMATECH.

13. I have authored or co-authored dozens of papers, reports, and presentations relating to semiconductor processing, and semiconductor equipment, fluid delivery components in semiconductor processing, and equipment reliability. I am additionally an inventor of four issued U.S. Patents, Nos. 6,679,476, related to a high-purity control valve; 6,204,174, related to semiconductor processing; 7,118,090, related to a high-purity fluid control valve; and 9,224,626 regarding design of heated wafer chucks for CVD and similar equipment.

14. For more aspects of my qualifications and publications, see my CV attached hereto as Exhibit 1 Veeco0001955-01974 (Alexander D. Glew, Ph.D., P.E. Curriculum Vitae).

15. I am familiar with and understand the concept in patent law of "infringement" of a patent, which is satisfied when all of the elements or limitations stated in a particular patent claim are found to be present in an accused infringing device or product.

16. I have reviewed the utility patent asserted in this matter, Veeco's U.S. Patent No. 6,726,769 (the '769 patent) and other materials which are cited in the Motion for Preliminary Injunction and this declaration. Based on my background and experience, I am competent to provide expert opinions on the claims of the '769 patent and whether or not certain products infringe those claims.

17. I am currently compensated for my time at the rate of \$515 per hour. My compensation does not depend on either the findings of my investigation or the outcome of the case.

### **Overview of MOCVD Wafer Carrier Technology**

18. Advances in semiconductor manufacturing, in particular relating to Light Emitting Diode ("LED") technology, today revolves around the ability to efficiently manufacture higher quality, lower cost, smaller, faster, and environmentally friendly semiconductor components.

19. Today, these components are made primarily by using specialized reactors to process "wafers" of sapphire ( $\text{Al}_2\text{O}_3$ ), silicon carbide ( $\text{SiC}$ ), silicon, and other materials. One way to process wafers and deposit material is by use of a process called Chemical Vapor Deposition (CVD). In one type of a CVD reactor system, a wafer is placed into a reactor and rotated at a designated speed while hot gasses meet at the surface of the wafer, react and deposit thereupon. Through this process, thin crystalline films are grown on the surface of the wafer, allowing the wafer to be further processed into fine electrical components. These processes may be used to form epitaxial layers (EPI) of semiconductor material on the underlying wafer. This allows one to use a wafer that does not have sufficient properties for forming for LEDs, by

deposition the EPI layer, and forming the LEDs thereupon. Simply, the EPI layer is superior to the wafer.

20. Metal Organic Chemical Vapor Deposition (“MOCVD”) reactors are a specific type of CVD reactor, often used in the manufacture of LEDs. Modern day LEDs are created using MOCVD reactors. The phrase “metal organic” refers to chemicals which have both an organic (carbon based) and metallic (metal or silicon) component used to deposit the films.

21. In a semiconductor processing chamber, a susceptor absorbs energy and then heats the wafer or wafer carrier holding multiple wafers during processing. It can both heat and hold (or chuck) a wafer or a wafer carrier. Prior to Veeco’s susceptorless wafer carrier inventions, manufactures processed individually wafers in a process chamber, generally known as single wafer processing. Alternatively, they processed multiple wafers at a time, known as batch processing, in a process chamber on either vertically oriented barrel shaped semi-permanent “wafer carriers” inside MOCVD reactors, in pancake reactors, or other batch configurations.<sup>2</sup> Reactors for single wafer uses resulted in higher quality depositions on the wafers, but processing wafers one at a time was not necessarily time efficient or cost effective. The batch systems used wafer carriers with multiple wafers for MOCVD reactors, and the carriers were placed into a reactor vertically because the methods for depositing materials in MOCVD reactors at the time involved horizontal flow of gasses. A separate device, the susceptor, held the rotating wafer carrier. An energy or heat source next to the susceptor heated it, which in turn heated the wafer carrier and wafers, while gases are applied to the surface of the wafer carrier which combine and react on the surface of the wafer.

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<sup>2</sup> S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, Vol. I: Process Technology, pp. 247-251 (2<sup>nd</sup> Ed. 2000), Ex. 3 at Veeco0001930-01934. A true and correct copy of excerpts of this reference is attached hereto as Exhibit 3 Veeco0001907-01934 (Wolf and Tauber reference); Peter Van Zant, *Microchip Fabrication: A practical Guide to Semiconductor Processing*, 359-394 (2000 4<sup>th</sup> Ed.). A true and correct copy of excerpts of this reference is attached hereto as Exhibit 10 Veeco0002029-02076 (Van Zant reference).

22. Each of these old methods had disadvantages. On one hand, single wafer CVD processing was slower compared to batch processing, and sacrificed throughput for quality. Manufacturing high quality wafers in mass was time consuming and required much equipment. Processing individual wafers would lead to the higher quality wafers, but production was slow and expensive. On the other hand, the batch systems, such as the prior vertical systems for manufacturing multiple wafers further did not achieve the process control of single wafer processing chambers and experienced lower yields. Further, in the susceptor systems of the past, there were significant efficiency and reliability losses created by the need to heat both the susceptor and the wafer carrier.

23. Aside from the process performance enhancements that a susceptorless system offers, such a system can reduce operating cost, service and maintenance, and increase tool uptime and availability. Opening a MOCVD process chamber to service it takes approximately one shift or eight hours. The process chamber is hot and must be cooled before opening, and has hazardous and toxic material. Furthermore, one must requalify the process after exposure to atmosphere. Semiconductor manufacturers using MOCVD must clean wafer carriers and susceptors as a part of routine maintenance every 1000  $\mu\text{m}$  of deposition, or approximately every 125 hours.<sup>3</sup> This translates to every five days in a factory running three shifts per day. The susceptorless design of the present invention negates the need to open the deposition chamber to clean the susceptor. Instead, wafer carriers in need of cleaning are removed from the separate loading position or vacuum load lock for cleaning, without opening the hot hazardous and delicate process chamber.

### **Veeco, SGL, and AMEC**

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<sup>3</sup> A. G. Thompson, W. Kroll, M.A. McKee, R.A. Stall, and P. Zawadski, *A Cost of Ownership Model for CVD Processes*, III-Vs Review, Vol. 8, No. 3, pp. 14-20 (1995), Ex. 4 at Veeco0001948-01954. A true and correct copy of this document is attached hereto as Exhibit 4 Veeco0001948-01954 (Thompson Kroll reference).

24. In the early 2000s, Veeco introduced new technology in the field of MOCVD reactors. Veeco's MOCVD Reactor featured an improved heater, gas flow flange apparatus, and very importantly, an improved wafer carrier, one that could function efficiently at high speeds of rotation.

25. A significant element of Veeco's MOCVD reactors are its innovative susceptorless wafer carriers, which are the subject of the '769 Patent. I have reviewed the '769 patent. I understand that Veeco has invested substantial resources into its wafer carrier design, and customers repeatedly purchase and use Veeco's MOCVD systems based on in part on Veeco's wafer carrier design. *See* Raman Decl. ¶¶ 9, 12-17.

26. I understand that SGL is one of Veeco's suppliers for susceptorless wafer carriers, and that SGL manufactures wafer carriers for Veeco and Veeco's customers for use in MOCVD systems. *See* Raman Decl. ¶¶ 30-32, 38.

27. I further understand that SGL now sells removable wafer carriers to one of Veeco's direct competitors in the MOCVD space, Advancement Micro Fabrication Equipment, Inc. (AMEC), for use in AMEC's MOCVD reactors. (the "Infringing Products").

28. The Infringing Products are loaded into automated MOCVD reactor systems, and are further designed to transport a plurality of wafers through the MOCVD process, much like how Veeco's wafer carriers operate. I have reviewed publicly available literature from SGL's website regarding the Infringing Products. *See* Rizzolo Decl. Ex. 2 Veeco0001987-02006 (SGL Semiconductor Brochure); Ex. 3 Veeco0002007-02008 (SGL Website).

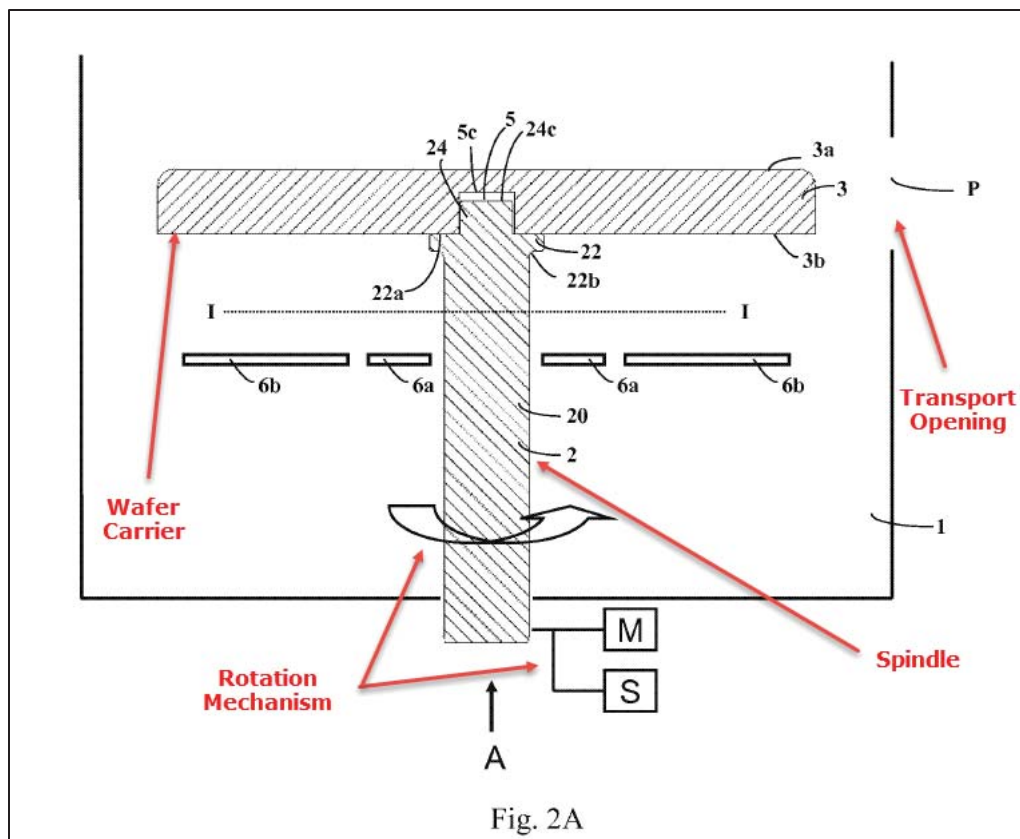
29. I understand that AMEC sells an MOCVD reactor system, the Prismo-D Blue<sup>TM</sup>. I have reviewed publicly available literature regarding AMEC's Prismo-D Blue<sup>TM</sup>. Copies of these documents are attached hereto as Exhibits 5-8 respectively: Veeco0001975-01980 (Qilong

Article); Veeco0001935-01942 (AMEC LpR Article); Veeco0001981-01986 (AMEC Prismo SSL Article); and Veeco0001884-01906 (AMEC Semicon Slides).

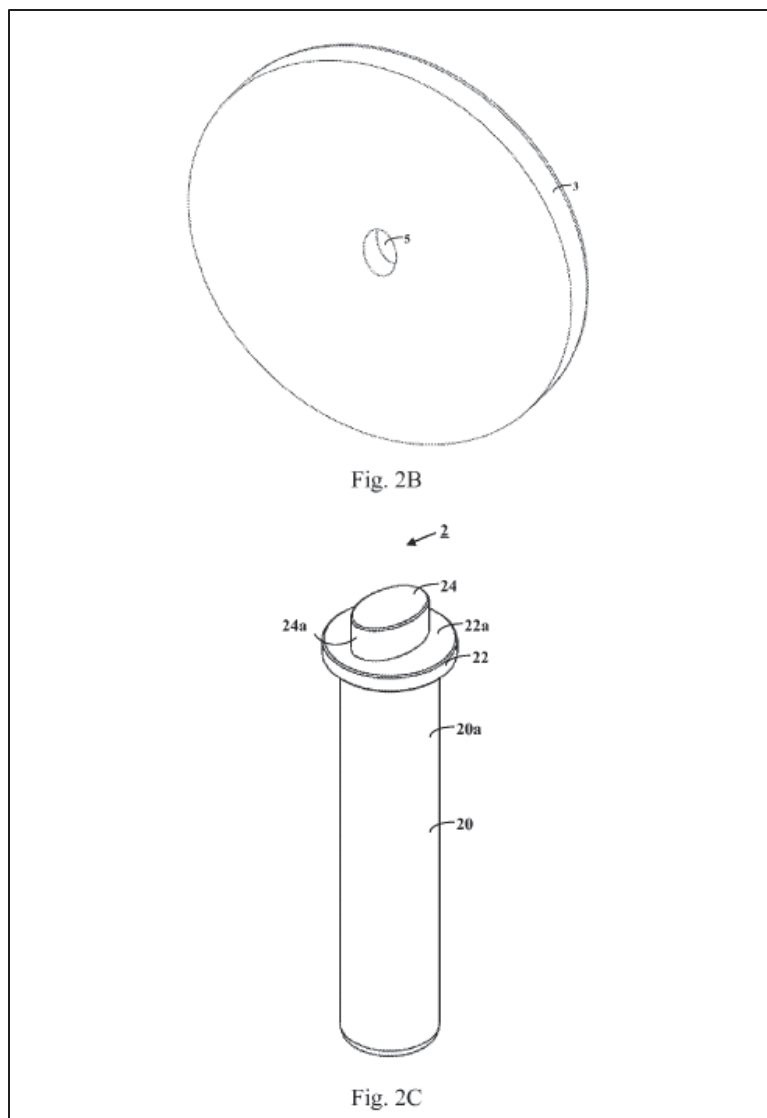
30. In my professional opinion based on publicly available information regarding the Prismo-D Blue<sup>TM</sup>, the Prismo-D Blue<sup>TM</sup> utilizes a “high-speed rotating mechanism” such as a rotatable spindle for rotating wafer carriers inside its reactors. Ex. 5 at Veeco0001977 (Qilong Article). The Prismo-D Blue<sup>TM</sup> further is an automated system with a “loading station” for wafer carriers. Ex. 6 at Veeco0001935-01936 (AMEC LpR Article); Ex. 7 at Veeco0001983-01984 (AMEC Prismo SSL Article). Wafer carriers are detachable from the rotating spindle assembly and transportable in the ordinary course of operation of the reactor. The Prismo-D Blue<sup>TM</sup> further shows multiple reactors attached to a single loading dock. Ex. 8 at Veeco0001892 (AMEC Semicon Slides). Further, In my opinion, and according to the evidence herein and described in my claim chart, Ex. 2, the only viable way to remove wafers that have been processed on an SGL wafer carriers in an AMEC MOCVD reactor is to transport the wafer carrier from the reactor so that the wafers and wafer carrier can cool down before wafer removal. Lastly, to the extent that it was possible to remove hot wafers from the hot wafer carrier in the process chamber, it would disadvantageous. Handling wafers, loading or unloading, to a wafer carrier in the process chamber requires wasted time during which wafer processing cannot occur, thereby reducing the availability of the tool for processing.

31. Thus, in my opinion, any wafer carrier used in the Prismo-D Blue<sup>TM</sup> reactor system would necessarily be detachable from the spindle. AMEC further submitted drawings and figures describing MOCVD reactor and wafer carrier technology in a published patent application, U.S. Application No. 13/681,768 (’768 Application). Rizzolo Decl. Ex. 4 Veeco0002268-02305 (AMEC’s ’768 Application). For example, AMEC’s ’768 Application

states, “Another object of the present application is to provide a supporter applicable in the 25 reactor, which can be detachably connected to a substrate carrier, and support the substrate carrier evenly and reliably while driving the substrate carrier to rotate evenly and reliably in substrate processing.” Rizzolo Decl. Ex. 4 at Veeco0002269 (AMEC’s ’768 Application). AMEC’s ’768 Application further states how “the substrate carrier 3 is transported into the reaction chamber 1 throughout the transport opening P by a robot ... is detachably placed on and supported by the supporter 2 . . . for [] substrate processing” and that “[a]fter the substrate processing is complete ... rotation of the rotary mechanism M is ceased ... [and] the substrate carrier 3 is detached from the support 2 by robot ... and then is sent out of the reaction chamber...” Rizzolo Decl. Ex. 4 at Veeco0002269 (AMEC’s ’768 Application). The figures disclosed by AMEC in the ’768 Application are further consistent with publicly available information regarding AMEC’s MOCVD systems, which further support my opinion. Rizzolo Decl. Ex. 4 at Veeco0002291-02299 (AMEC’s ’768 Application):

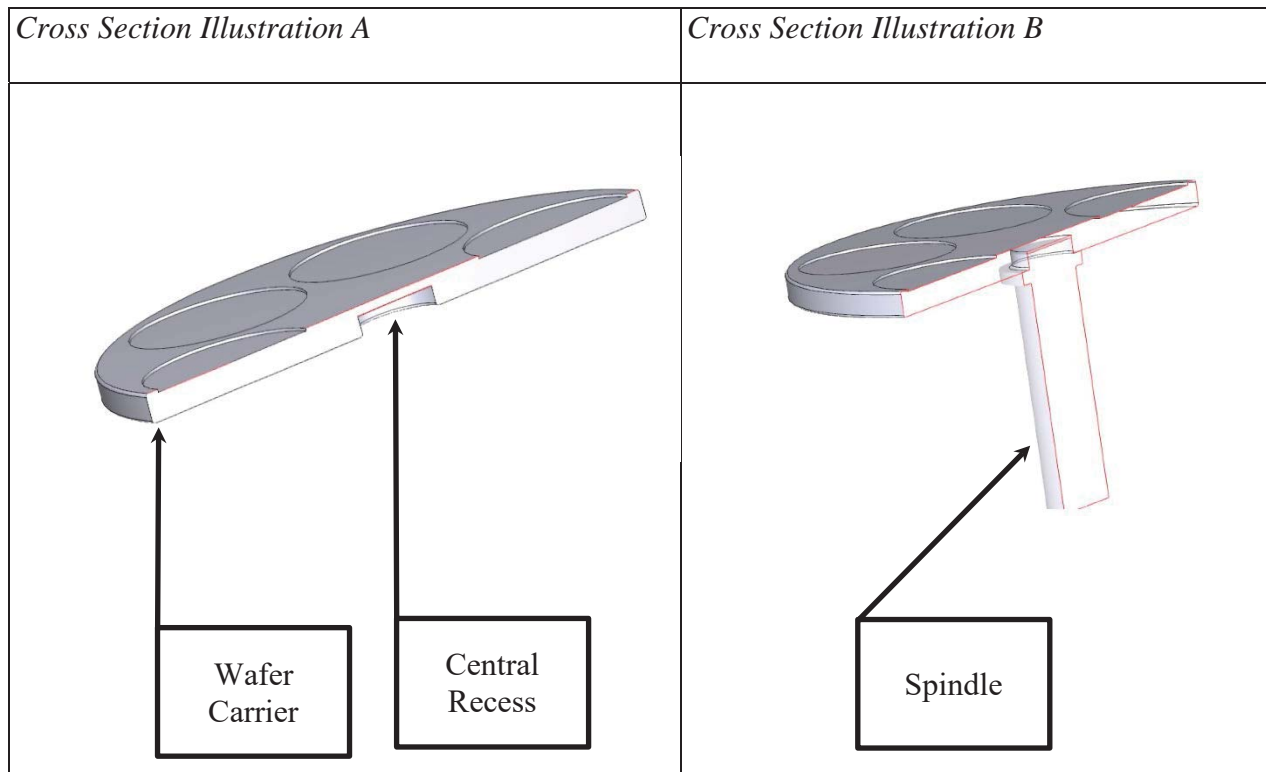


AMEC's '768 Application, Rizzolo Decl. Exhibit 4 at Veeco0002291 (annotated).



AMEC's '768 Application, Rizzolo Decl. Exhibit 4 at Veeco0002274.

32. The following annotated diagram, which I personally created, substantially depicts the structure and functionality of the Infringing Products based on my analysis of the publicly available documentation, including AMEC's '768 Application:



### Applicable Legal Understanding

33. In this section I describe my understanding of certain legal standards. I have been informed of these legal standards by Veeco's attorneys. I am not an attorney and I am relying only on instructions from Veeco's attorneys for these legal standards.

34. I have been informed and understand that the determination of infringement is a two-step process. First, the claims must be construed by the Court. Second, the infringing products or processes must be compared to the properly construed claims. I understand that in order to infringe a patent claim, an accused product or process must include each and every limitation recited in that patent claim.

35. I have been informed and understand that in order for plaintiff to obtain a preliminary injunction, plaintiff must establish that plaintiff is likely to succeed on the merits of the patent litigation, that plaintiff will suffer irreparable harm in the absence of preliminary

relief, and that the balance of equities and public interest weigh in favor of granting the injunction.

36. I am informed that the meaning of claim terms and infringement must be analyzed from the perspective of “one of ordinary skill in the art” involved in the same field as the Patents-in-Suit at the time of the invention.

37. I understand that, in construing the claims, claim terms are generally given their “plain and ordinary meaning.”

#### **Level of a Person of Ordinary Skill In The Art and Claim Construction**

38. In my opinion, one of ordinary skill in the art of the '769 Patent at the time of the invention would have a bachelor's degree in electrical, chemical, or mechanical engineering, materials science, or a comparable degree, and two to three years of work experience in semiconductor equipment design, semiconductor fabrication or CVD/MOCVD systems.

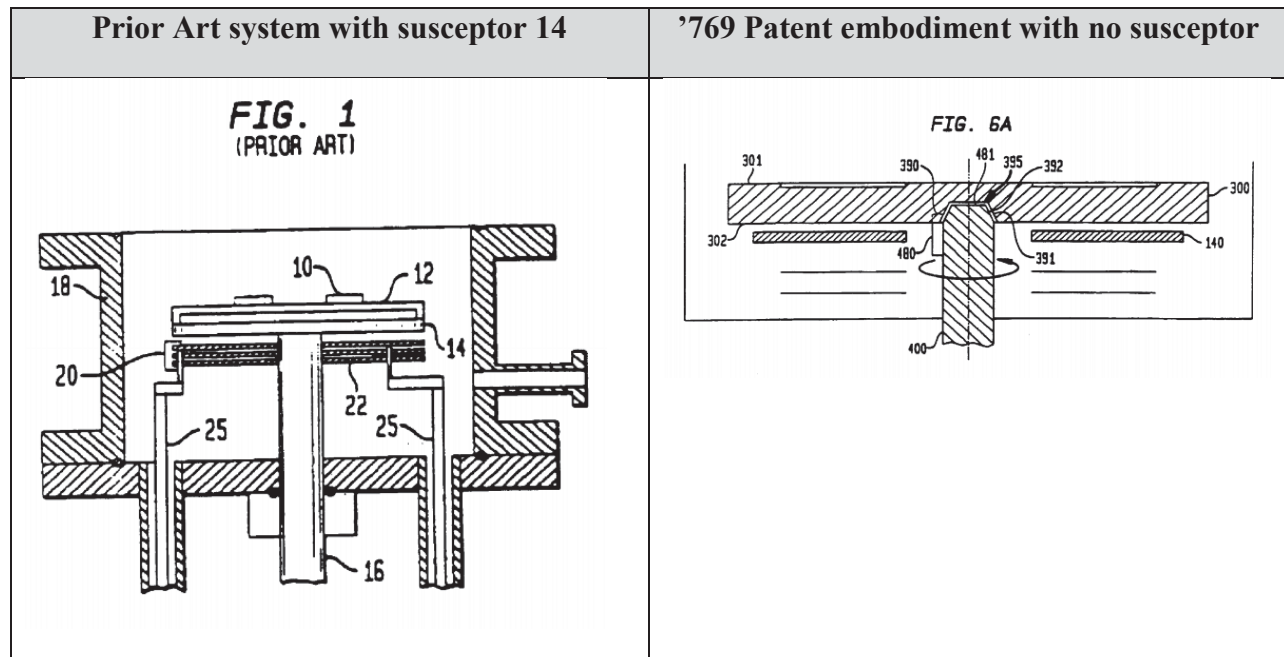
39. The terms of the '769 Patent are not especially technical. They have a plain and ordinary meaning to those skilled in the field.

#### **Overview of the '769 Patent**

40. The '769 Patent is titled “Susceptorless reactor for growing epitaxial layers on wafers by chemical vapor deposition” and was issued on April 27, 2004. It discloses “... a novel CVD reactor in which the wafer carrier is placed on the rotatable spindle without a susceptor, and a related method of growing epitaxial layers in a CVD reactor.” '769 Patent Col. 4:8-11. The invention also describes that the wafer carrier is removable mounted on the rotatable spindle, using the center of gravity to increase stability. “When the wafer carrier is mounted onto the upper end of the spindle, the upper end of the spindle is inserted into the central recess in the bottom surface of the wafer carrier. The insertion provides a point of contact between the

spindle and the wafer carrier, allowing the wafer carrier to be supported by the spindle. To improve the rotational stability of the wafer carrier, the point of contact between the spindle and the wafer carrier having the highest elevation is located above the center of gravity of the wafer carrier.” ’769 Patent Col. 5:58-67. Further, “The wafer carrier is mounted in a manner that allows it to be readily removed from the upper end of the spindle.” ’769 Patent Col. 5:34-36.” For example, Claim 1 requires that the wafer carrier be detachable in that it can be in a position such that the rotating spindle is no longer inserted in it.

41. The ’769 Patent is generally directed to wafer carrier devices, often used for growing epitaxial layers on substrates such as wafers in CVD systems. (*See, e.g.* Col. 1:18-20). Figure 1 of the ’769 shows a prior art system with a semi-permanent susceptor 14, a wafer carrier (holder) 12, heaters 22 and wafers 10. The system transfers heat radiantly from the heaters 22 to the semi-permanent susceptor 14, then to the wafer carrier 12, and lastly to the wafer 10. Figure 6A of the ’769 patent shows an embodiment of the present invention. It describes a Veeco wafer carrier invention of the ’769 with a wafer carrier 300 and heaters 140. It advantageously transfers radiant heat directly from the heaters to the removable wafer carrier, without an intervening susceptor, then to the wafers. The wafer carrier design is not permanently mounted on a susceptor. Instead, the wafer carrier is removable from the spindle such that the spindle is not inserted in the wafer carrier. Further, in some embodiments, the wafer carrier enters and leaves the process chamber with the wafers; while it is in the chamber, it is temporarily mounted to the spindle to heat and hold the wafers until processing is complete. Subsequent to processing, the wafer carrier is moved from the processing chamber to the loading area, along with the wafers. A comparison of these two patent figures is set forth below:



42. The inventors explain that this susceptorless configuration optimizes MOCVD systems in a number of ways: The rotational stability of the claimed wafer carrier design reduces vibration; the absence of a susceptor reduces thermal inertia and the temperature gradient between the wafer and heat source, which reduces weight from not having a susceptor, that consequently reduces strain on the spindle and increases the lifetime of the reactor; and the elimination of the contact between the susceptor and the wafer carrier results in better wafer production uniformity. *See* '769 Patent Col. 10:9-32.

43. Veeco's system allows for certain advantages, such as superior cleanliness and increased system availability or "tool uptime." Other systems utilize a semi-permanent mounted susceptor in the process chamber. The high temperatures and chemical exposure in the CVD process chamber wear and degrade the susceptor. The service personnel must periodically remove the susceptors for service. This requires opening the CVD process chambers and replacing the susceptors. This service results in excessive downtime for the CVD process tool, during which time no production can occur. The downtime is expensive for the factory, often far

more expensive than the parts or service call. Also, periodically, the CVD chambers need to be cleaned. The vast majority, in excess of 90% of product yield loss, is due to particles that contaminate the product.<sup>4</sup> Even if the susceptor does not need to be replaced, but merely cleaned, the resulting service call results in significant machine downtime and loss of production. After opening a process chamber, one must requalify the process by running sample processing and measuring the resulting output quality. Requalifying production on a CVD process chamber that has been opened and serviced is part of the time and expense of changing or cleaning a susceptor in a CVD chamber.

44. A susceptorless design allows one to clean or replace the wafer carrier without opening the CVD chamber. It is significantly easier to open a transfer chamber, where wafer loading takes place, than a processing chamber.

45. Veeco's invention of combining the susceptor and wafer carrier together into a transportable into a single unit that is easily transportable on and off a rotatable spindle in the MOCVD reactor was a fundamental improvement in the field. The wafer carriers have improved lifecycles and allow for longer uninterrupted processing of wafers in the MOCVD systems for longer periods of time, ultimately resulting in the superior performance of Veeco's reactors over its legitimate competitors. I understand that before SGL began selling wafer carriers to Veeco's competitor AMEC, no other company offered an MOCVD reactor that operated autonomously with high speeds of rotation.

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<sup>4</sup> Kirk J. Mikkelsen, *Transport and Storage Wafer Carrier Cost of Ownership*, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 45-49 (1995) Ex. 9 at Veeco0001943-01947 (Mikkelsen reference). A true and correct copy of this document is attached hereto as Exhibit 9 Veeco0001943-01947 (Mikkelsen reference).

**SGL Infringes Claims 1-5, 10, 13-16 of the '769 Patent**

46. Based on my analysis herein and the attached claim chart (which I hereby incorporate into my declaration by reference as Exhibit 2, I conclude the Infringing Products infringe claims of the '769 Patent and that Veeco is likely to succeed on the issue of infringement.

47. Claim 1 of the '769 Patent recites the following:

An apparatus for supporting and transporting at least one wafer in a CVD reactor having a rotatable spindle, said apparatus comprising:  
a top surface having at least one cavity for retaining said at least one wafer, and  
a bottom surface having a central recess adapted for detachably inserting an upper end of said rotatable spindle;  
said apparatus being transportable, in the normal course of operation of the CVD reactor, between a position in which said spindle is inserted into said central recess for rotation therewith and a position detached from said spindle.

48. It is my opinion that the phrase “An apparatus for supporting and transporting at least one wafer in a CVD reactor having a rotatable spindle, said apparatus comprising”—whether or not it is viewed as a limitation of the claim—is met by the Infringing Products. The Infringing Products are used and sold for supporting and transporting at least one wafer in a CVD reactor with a rotatable spindle. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-4 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application).

49. It is my opinion that the Infringing Products meet the limitations of Claim 1. The Infringing Products further have a top surface having at least one cavity for retaining a substrate wafer. Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). In my professional opinion based on years of experience with similar CVD systems, the Infringing

Products have a bottom surface having a central recess adapted for detachably inserting an upper end of a rotatable spindle. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). In my professional opinion based on years of experience with similar CVD systems, the Infringing Products, in the normal course of operation of a CVD reactor, are transportable between a position where a spindle is inserted into its central recess and a position detached from the spindle. Exs. 6-8 Veeco0001935-01942 (AMEC LpR Article); Veeco0001981-01986 (AMEC Prismo SSL Article); Veeco0001884-01906 (AMEC Semicon Slides); Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application).

50. My analysis regarding Claim 1 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

51. Claim 2 of the '769 patent recites the following:

The apparatus of claim 1, wherein said central recess extends from said bottom surface of said apparatus to a recess end point, which is located at a lower elevation than said top surface of said apparatus and at a higher elevation than said bottom surface of said apparatus.

52. It is my opinion that the Infringing Products meet the additional limitations of Claim 2. In my professional opinion based on years of experience with similar CVD systems, the central recess of the Infringing Products extends from the bottom surface to a recess endpoint that is at a lower elevation than the top surface of the Infringing Products and at a higher elevation than the bottom surface of the Infringing Products. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-4 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website);

Veeco0002268-02305 (AMEC's '768 Application). My analysis regarding Claim 2 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

53. Claim 3 of the '769 Patent recites the following:

The apparatus of claim 2, wherein said central recess comprises a recess wall and an end surface, said recess wall extending from said bottom surface of said apparatus toward said end surface of said central recess.

54. In my professional opinion based on years of experience with similar CVD systems, the central recess of the Infringing Products comprises a recess wall and end surface, where the recess wall extends from the bottom surface toward the end surface of the central recess. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). My analysis regarding Claim 3 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

55. Claim 4 of the '769 Patent recites the following:

The apparatus of claim 3, wherein said recess wall terminates at said end surface.

56. In my professional opinion based on years of experience with similar CVD systems, the recess wall of the central recess in the Infringing Products terminates at the end surface. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). My analysis regarding Claim 4 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

57. Claim 5 of the '769 Patent recites the following:

The apparatus of claim 4, wherein said end surface contains said recess end point.

58. In my professional opinion based on years of experience with similar CVD systems, the end surface of the Infringing Products' central recess contains a recess end point. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). My analysis regarding Claim 5 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

59. Claim 10 of the '769 Patent recites the following:

The apparatus of claim 3 having a center of gravity located below said end surface of said central recess.

60. In my professional opinion based on years of experience with similar CVD systems, the center of gravity (COG) of the Infringing Products is below the end surface of the central recess. Exs. 5-6 Veeco0001975-01980 (Qilong Article); Veeco0001935-01942 (AMEC LpR Article); Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website). My analysis regarding Claim 10 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2. The center of gravity is at approximately half way through the thickness of the wafer carrier shown in the chart in Exhibit 2 at Claim 1, *Cross Sectional Illustrational A*, for the following reasons: the wafer pockets are small, and the central recess is small compared to the mass of the wafer carrier as a whole. This is true for any wafer carrier that is substantially shaped like a disk. A central recess that is deeper than half the depth of the wafer carrier yields a center of gravity that is below the end surface of the central recess. Exhibit 2 at Claim 10. The deeper the central

recess, the more the wafer carrier is able to stay mounted on the spindle during operation without permanent attachment. Additionally, the COG being below the endpoint of the central recess increases the stability and provides some additional restoring force if the wafer carrier were to tip during mounting or other operations, somewhat similar to a boat with a deep keel righting itself. Exhibit 2 at Claim 10. For example, note that the COG of the wafer carrier is close to but below its center line (the halfway point between the top and bottom surface) in the scaled CAD model illustration given in the chart, whereas the end of the recess is above the center line, allowing for stability of the Infringing Products during rotation. Exhibit 2 at Claim 1, *Cross Sectional Illustrational A*.

61. Claim 13 of the '769 Patent recites the following:

The apparatus of claim 1, wherein said top surface and said bottom surface of said apparatus are substantially parallel to each other.

62. The Infringing Products have a top surface and a bottom surface substantially parallel to each other. Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). My analysis regarding Claim 13 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

63. Claim 14 of the '769 Patent recites the following:

The apparatus of claim 1, wherein said top surface has a plurality of cavities for retaining a plurality of wafers.

64. The top surface of the Infringing Products have a plurality of cavities for retaining a plurality of wafers. Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768

Application). My analysis regarding Claim 14 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

65. Claim 15 of the '769 Patent recites the following:

The apparatus of claim 1 having a substantially round shape.

66. The Infringing Products have a substantially round shape. Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website); Veeco0002268-02305 (AMEC's '768 Application). My analysis regarding Claim 15 is further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

67. Claim 16 of the '769 Patent recites the following:

The apparatus of claim 1, which is made of graphite.

68. The Infringing Products are made of graphite. Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website). My analysis is regarding Claim 16 further detailed in the attached claim charts, which I hereby incorporate into my declaration by reference as Exhibit 2.

69. Finally, I understand that in its marketing literature, SGL has touted the Infringing Products' thermal conductivity, reliability, efficiency, increased chip yield, and improved quality of wafers produced. Rizzolo Decl. Exs. 2-3 Veeco0001987-02006 (SGL Semiconductor Brochure); Veeco0002007-02008 (SGL Website). In my opinion, these are features that are made possible using claims 1-5, 10, and 13-16 of the '769 Patent.

### **Exhibits**

70. Attached hereto as Exhibit 1 Veeco0001955-01974 (Alexander D. Glew, Ph.D., P.E. Curriculum Vitae) is a copy of my Curriculum Vitae ("CV").

71. Attached hereto as Exhibit 2 is a copy of an infringement claim chart I prepared (which I hereby incorporate into my declaration by reference).

72. Attached hereto as Exhibit 3 Veeco0001907-01934 (Wolf and Tauber reference) is a true and correct copy of excerpts from a reference entitled “Silicon Processing for the VLSI Era.” S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, Vol. I: Process Technology, 247-251 (2<sup>nd</sup> Ed. 2000).

73. Attached hereto as Exhibit 4 Veeco0001948-01954 (Thompson Kroll reference) is a true and correct copy of excerpts from a reference entitled “A Cost of Ownership Model for CVD Processes.” A. G. Thompson, W. Kroll, M.A. McKee, R.A. Stall, and P. Zawadski, *A Cost of Ownership Model for CVD Processes*, III-Vs Review, Vol. 8, No. 3, 14-20 (1995).

74. Attached hereto as Exhibit 5 Veeco0001975-01980 (Qilong Article) is a true and correct copy of an article entitled “Effect of Hydrogen Carrier Gas on AlN and AlGa<sub>N</sub> Growth in AMEC Prismo D-Blue MOCVD Platform.” Qilong Bao, Article, *Effect of hydrogen carrier gas on AlN and AlGa<sub>N</sub> growth in AMEC Prismo D-Blue® MOCVD platform*, Journal of Crystal Growth (June 2015) (available online at [https://www.researchgate.net/publication/273789925\\_Effect\\_of\\_hydrogen\\_carrier\\_gas\\_on\\_AlN\\_and\\_AlGa<sub>N</sub>\\_growth\\_in\\_AMEC\\_Prismo\\_D-BlueR\\_MOCVD\\_platform?el=1\\_x\\_3&enrichId=rgreq-c870e90b-913b-4c07-a3bc-643093ac6d87&enrichSource=Y292ZXJQYWdlOzI3Mzc4OTkyNTtBUzoyMTA0NDExNDI4MzcyNTNAMTQyNzE4NDQ4Njg1NQ%3D%3D](https://www.researchgate.net/publication/273789925_Effect_of_hydrogen_carrier_gas_on_AlN_and_AlGaN_growth_in_AMEC_Prismo_D-BlueR_MOCVD_platform?el=1_x_3&enrichId=rgreq-c870e90b-913b-4c07-a3bc-643093ac6d87&enrichSource=Y292ZXJQYWdlOzI3Mzc4OTkyNTtBUzoyMTA0NDExNDI4MzcyNTNAMTQyNzE4NDQ4Njg1NQ%3D%3D)).

75. Attached hereto as Exhibit 6 Veeco0001935-01942 (AMEC LpR Article) is a true and correct copy of an article entitled “MOCVD Platform for Cost-Effective Production of GaN-based HB LEDs.” LED professional Review, Article, *MOCVD Platform for Cost-Effective*

*Production of GaN-based HB LEDs* (Oct. 7, 2016) (available online at <https://www.led-professional.com/resources-1/articles/mocvd-platform-for-cost-effective-production-of-gan-based-hb-leds-by-advanced-micro-fabrication-equipment-inc>).

76. Attached hereto as Exhibit 7 Veeco0001981-01986 (AMEC Prismo SSL Article) is a true and correct copy of an article entitled “A New MOCVD Platform, Prismo D-Blue, for High-throughput GaN LED Production.” Advanced Micro-Fabrication Equipment Inc., Product Introduction, *A New MOCVD Platform, Prismo D-Blue™, for High Throughput GaN LED Production* (published in Solid State Lighting (ChinaSSL), 2013 10th China International Forum on Solid State Lighting).

77. Attached hereto as Exhibit 8 Veeco0001884-01906 (AMEC Semicon Slides) is a true and correct copy of an AMEC presentation entitled “Prismo D-Blue, a New MOCVD Platform for GaN-based HB LED Production.” Advanced Micro-Fabrication Equipment Inc., *Prismo D-Blue™, a New MOCVD Platform for GaN-based HB LED Production*, Semicon PowerPoint Presentation (2013). I understand that this presentation was presented at the 2013 LED Technology Forum on Taiwan by Dr. Zhiyou Du, Chief Operating Officer and GM of the MOCVD Product Group at AMEC.<sup>5</sup>

78. Attached hereto as Exhibit 9 Veeco0001943-01947 (Mikkelsen reference) is a true and correct copy of an article entitled “Transport and Storage Wafer Carrier Cost of Ownership.” Kirk J. Mikkelsen, *Transport and Storage Wafer Carrier Cost of Ownership*, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 45-49 (1995).

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<sup>5</sup> See AMEC Website, *AMEC COO & MOCVD PRODUCT GROUP GM TO PRESENT AT THE 2013 LED TECHNOLOGY FORUM IN TAIWAN*, available online at <http://www.amec-inc.com/news/Events.php>. Copy attached as Rizzolo Decl. Ex. 5 Veeco0002310.

79. Attached hereto as Exhibit 10 Veeco0002029-02076 (Van Zant reference) is a true and correct copy of excerpts from a reference entitled “Silicon Processing for the VLSI Era.” Peter Van Zant, *Microchip Fabrication: A practical Guide to Semiconductor Processing*, 359-394 (2000 4<sup>th</sup> Ed.).

I declare under penalty of perjury under the laws of the State of New York and the United States of America that the foregoing is true and correct to the best of my information, knowledge, and belief.

A handwritten signature in brown ink that reads "Alexander D. Glew". The signature is written in a cursive style with a large, stylized 'A' and 'G'.

DN:  
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engineering.com  
Date: 2017.07.21  
13:20:57 -07'00'

Dated: July 21, 2017

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Dr. Alexander Glew

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